Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Withdrawn) A floating gate memory array, comprising:

a) an array of floating gate memory cells,

b) a source line coupled to cells in a row of said array,

c) a word line coupled to control gates of transistors of said memory cells in the row of said array,

d) a read bit line and a program bit line connecting between said memory cells in each column of said array.

2. (Withdrawn) The memory array of claim 1, wherein said word line for the row of memory cells in said array is segmented and each segment is driven by a word line driver to allow simultaneous memory operations on a number of cells fewer in quantity than that of a complete row.

3. (Withdrawn) The memory array of claim 1, wherein each row of memory cells in said array is coupled to a unique source line.

4. (Withdrawn) The memory array of claim 3, wherein said read bit line and said program bit line are merged into one bit line connecting between memory cells in a column.

5. (Withdrawn) The memory array of claim 1, further comprising:

a) a split gate read transistor and a split gate program transistor forming said memory cells,

b) a floating gate of said read transistor connected to the floating gate of said program transistor and thereby merging the two floating gates,

c) said read bit line connected to a drain of the read transistor,

d) said program bit line connected to the drain of the program transistor.

6. (Withdrawn) The memory array of claim 5, wherein said program transistor is given an extra implant to increase threshold voltage to prevent punch-through.

7. (Withdrawn) The memory array of claim 1, further comprising:

a) a split gate read transistor, a split gate program transistor and a spare split gate transistor forming said memory cells,

b) a floating gate of said read transistor connected to the floating gate of said program transistor and thereby merging the two floating gates,

c) said read bit line connected to a drain of the read transistor,

d) said program bit line formed by a first program bit line and a second program bit line,

e) said first program bit line connected to the drain of the split gate program transistor,

f) said second program bit line connected to the drain of the spare split gate transistor.

8. (Withdrawn) The memory array of claim 7, wherein said memory cell in an adjacent row of a column is formed with the first program bit line connected to the drain of the spare split gate transistor and the second program bit line connected to the drain of the split gate program transistor.

9. (Withdrawn) The memory array claim 7, wherein said program transistor, said read transistor and said spare transistor are formed with a thin cell.

10. (Withdrawn) The memory array of claim 7, wherein said memory cells are formed with said split gate read transistor and said split gate program transistor, whereby the first program bit line is connected to the drain of said program transistor and the second program bit line is connected to the program transistor in said memory cell of an adjacent row of the column.

11. (Withdrawn) The memory array of claim 10, wherein said program transistor is formed with a thin cell and said read transistor is formed with a fat cell.

12. (Withdrawn) A method for re-write if disturbed, comprising:

a) loading input address and data into a page buffer,

b) reading out original data from an address location of an array to a page buffer,

c) erasing said address location, verifying the erasing of said address location, and erasing bytes failing verification,

d) programming said address location, verifying the programming of said address location, programming bytes failing programming,

e) verifying data in unchanged portion of said address location

f) ending if verification of unchanged portion of said address location is passed, else re-write failed locations.

13. (Withdrawn) The method of claim 12, wherein verifying the erasing of said address location uses a verification read of a marginal "1".

14. (Withdrawn) The method of claim 12, wherein verifying the programming of said address location uses a verification read of a marginal "0".

15. (Previously Presented) A memory array utilizing cells with one split gate transistor, comprising:

an array of one transistor split gate cells arranged into rows and columns in which even addressed cells are located in a first row of cells and odd addressed cells are located in a second row of cells,

a split source line connected to said even and odd addressed cells,

said first row being connected with a first word line and said second row being connected with a second word line, and

said cells in one of said columns being connected to a bit line.

16. (Previously Presented) The memory array of claim 15, wherein said row of even addressed cells is connected to a first source line and said row of odd addressed cells is connected to a second source line.

17. (Currently Amended) The memory array of claim 15, wherein ~~said first and second rows are connected with said first and second word lines by segmenting~~ each of said first and second word lines is divided into word line segments.

18. (Currently Amended) The memory array of claim 17, wherein each word line segment is driven with [[a]] an associated word line driver ~~where~~ and each word line segment is shorter in length than said row.

19. (Previously Presented) A memory array utilizing cells with two split gate transistors, comprising:

an array of two transistor split gate cells arranged into rows and columns in which even addressed cells are located in a first row of cells and odd addressed cells are located in a second row of cells,

a split source line connected to said even and odd addressed cells,

said first row being connected with a first word line and said second row being connected with a second word line, and

said cells in one of said columns being connected to a program bit line and a read bit line.

20. (Previously Presented) The memory array of claim 19, wherein the two transistor split gate cells comprise a first floating gate of a first split gate transistor coupled with a second floating gate of a second split gate transistor.

21. (Previously Presented) The memory array of claim 19, wherein said row of even addressed cells is connected to a first source line, and said row of odd addressed cells is connected to a second source line.

22. (Currently Amended) The memory array of claim 19, wherein ~~said first and second rows are connected with said first and second word lines by segmenting~~ each of said first and second word lines is divided into word line segments.

23. (Currently Amended) The memory array of claim 22, wherein each word line segment is driven with [[a]] an associated word line driver ~~where~~ and each word line segment is shorter in length than said row.

24. (Previously Presented) A memory array utilizing cells with three split gate transistors, comprising:

an array of cells containing three split gate transistors arranged into rows and columns in which even addressed cells are located in a first row of cells and odd addressed cells are located in a second row of cells,

a floating gate shared between a first and a second split gate transistor of said three split gate transistors,

a source line shared between said even and odd addressed cells,

said first row being connected with a first word line and said second row being connected with a second word line, and

said cells in one of said columns being connected with a first program bit line, a second program bit line and a read bit line.

25. (Previously Presented) The memory array of claim 24, wherein:

a) a first cell in a first row of one of the columns includes said first transistor, said second transistor and a third transistor,

b) a second cell in a second row of said column includes said first transistor, said second transistor, and said third transistor,

c) said first program bit line is connected to said first transistor in said first row and said third transistor in said second row,

d) said second program bit line is connected to said third transistor in said first row and said first transistor in said second row, and

e) said read bit line is connected to said second transistor of said first row and to said second transistor of said second row.

26. (Previously Presented) The memory array of claim 24, wherein said first and second rows are connected with said first and second word lines by segmenting said first and second word lines.

27. (Original) The memory array of claim 26, wherein each word line segment is driven with a word line driver where each segment is shorter in length than said row.

28. (Original) The memory array of claim 26, wherein said first, second and third transistors are thin transistors.

29. (Previously Presented) A memory array utilizing cells with two split gate transistors, comprising:

an array of cells containing two split gate transistors arranged into rows and columns in which even addressed cells are located in a first row of cells and odd addressed cells are located in a second row of cells,

a floating gate shared between a first and a second split gate transistor of said two split gate transistors,

a source line shared between said even and odd addressed cells,

said first row being connected with a first word line and said second row being connected with a second word line,

said cells in one of said columns being connected with a first program bit line, a second program bit line and a read bit line.

30. (Previously Presented) The memory array of claim 29, wherein:

a) a first cell in a first row of one of said columns includes said first transistor and said second transistor,

b) a second cell in a second row of said column includes said first transistor and said second transistor,

c) said first program bit line is connected to said first transistor in said first row,

d) said second program bit line is connected to said first transistor in said second row,

e) said read bit line is connected to said second transistor of said first row and to said second transistor of said second row.

31. (Previously Presented) The memory array of claim 29, wherein said first and second rows are connected with said first and second word lines by segmenting said first and second word lines.

32. (Original) The memory array of claim 31, wherein each word line segment is driven with a word line driver where each segment is shorter in length than said row.

33. (Original) The memory array of claim 31, wherein said first transistor is a thin transistor and said second transistor is a fat transistor.

34. (Previously Presented) A memory array containing cells with two split gate transistors, comprising:

an array of cells containing two split gate transistors arranged in rows and columns,

a floating gate shared between a first and a second split gate transistor of said two split gate transistors,

means for increasing the threshold voltage of said first split gate transistor,

a source line shared between said even and odd addressed cells,

said first row being connected with a first word line and said second row being connected with a second word line,

said cells in one of said columns being connected with a program bit line and a read bit line.

35. (Original) The memory array of claim 34, wherein the means for increasing the threshold voltage of said first split gate transistor uses an added implantation.

36. (Original) The memory array of claim 34, wherein the means for connecting between cells in a column further comprising:

a) a first cell in a first row of a column containing said first transistor and said second transistor,

b) a second cell in a second row of said column containing said first transistor and said second transistor,

c) said program bit line connecting to said first transistor in said first row and said second row,

d) said read bit line connecting to said second transistor of said first row and to said second transistor of said second row.

37. (Currently Amended) The memory array of claim 34, wherein ~~the means for connecting said first and second rows with said first and second word lines is done by segmenting~~ each of said first and second word lines is divided into word line segments.

38. (Currently Amended) The memory array of claim 37, wherein each word line segment is driven with [[a]] an associated word line driver ~~where~~ and each word line segment is shorter in length than said row.

39. (Withdrawn) A method for re-writing disturbed cells, comprising:

a) a means for loading a page buffer with input addresses and data,

b) a means for reading data from a memory location into said page buffer,

c) a means for erasing said address location and re-erasing those bytes failing verification of said erasing,

d) a means for programming said memory location and re-programming those bytes failing verification of said programming,

e) a means for verifying data in unchanged portion of said memory location and ending process if verification is true, else return to step c) to re-program data.

40. (Withdrawn) The method of claim 39, wherein verification of said erasing uses a read for a marginal "1".

41. (Withdrawn) The method of claim 39, wherein verification of said programming uses a read of for a marginal "0".